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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/742,288	12/22/2000	Richard P. Modelski	P 0270187 NOR-13179BA	8168

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PILLSBURY WINTHROP LLP
2475 HANOVER STREET
PALO ALTO, CA 94304-1114

EXAMINER	
DENNISON, JERRY B	

ART UNIT	PAPER NUMBER
2143	

DATE MAILED: 09/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/742,288	MODELSKI ET AL.	
	Examiner	Art Unit	
	J. Bret Dennison	2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Action is in response to Application Number 09/742,288 received on 22 December 2000.

2. Claims 1-19 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Cho (U.S. Patent Number 6,599,099).

3. Regarding claims 1 and 6, Cho discloses a method for manipulating data in a processor, the method comprising:

performing a conditional shift operation on an index register based on the condition of a carry flag, the condition of the carry flag having been set by a previous arithmetic operation (Cho, col. 10, line 33 through col. 11, line 10, Cho discloses performing a shift operation on an index register based on a flag value); and

performing an indexed load operation using an index register (Cho, col.11, lines 4-10).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho as applied to claim 1, in view of Narad et al. (U.S. Patent Number 6,157,955) and Gobuyan et al. (U.S. Patent Number 5,917,821).

4. Regarding claim 2, Cho teaches the limitations, substantially as claimed, as described in claim 1. Cho does not explicitly state:

transferring data from an input buffer to a packet task;

dispatching the data from the packet task manager to an analysis machine;

classifying the data in the analysis machine; and

implementing a binary search in the analysis machine.

In an analogous art, Narad teaches transferring data from an input buffer to a packet task manager (Narad, col. 9, lines 11-26, col. 15, lines 14-18);

dispatching the data from the packet task manager to an analysis machine (Narad, col. 36, lines 40-45);

classifying the data in the analysis machine (Narad, col. 37, lines 14-26);

In an another analogous art, Gobuyan teaches using a binary search on addresses for analysis (Gobuyan, col. 9. lines 34-40).

Therefore it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Cho by the teachings of Narad and Gobuyan to provide a platform for accelerated network infrastructure applications by speeding up searches through lists of unknown addresses.

5. Regarding claim 4, Cho, Narad, and Gobuyan disclose the limitations, substantially as claimed, as described in claim 2, including transferring the data after modifying and forwarding to an output buffer (Narad, col. 9, lines 1-27).

Claims 3, 7, 10-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho in view of Narad et al. (U.S. Patent Number 6,157,955).

6. Regarding claim 3, Cho discloses the limitations, substantially as claimed, as described in claim 1. However, Cho does not explicitly state further comprising modifying and forwarding the data in a packet manipulator. In an analogous art, Narad teaches modifying and forwarding the data in a packet manipulator (Narad, col. 31, lines 29-32 and lines 35-53).

7. Regarding claim 7, Cho teaches the limitations, substantially as claimed, as described in claim 6. Cho does not explicitly state:

an analysis machine having multiple pipelines, wherein one pipeline is dedicated to directly manipulating individual data bits of a bit field (Narad, col. 3, lines 56-65, col. 24, lines 50-64, col. 59, lines 39-50);

a packet task manager operationally connected to said analysis machine (Narad, col. 14, lines 53-63); and,

a packet manipulator operationally connected to said analysis machine (Narad, col. 59, line 39 through col. 60, line 10).

Therefore it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Cho by the teachings of Narad to provide a platform for accelerated network infrastructure applications by speeding up searches through lists of unknown addresses.

8. Regarding claim 10, Cho teaches the limitations, substantially as claimed, as described in claim 7 including:

a packet task manager operationally connected to said analysis machine (Narad, col. 14, lines 53-63);

a packet manipulator operationally connected to 'said analysis-machine (Narad, col. 59, line 39 through col. 60, line 10); and

a global access bus including a master request bus and a slave request bus separated from each other and pipelined (Narad, col. 36, lines 40-45).

9. Regarding claim 11, Cho teaches the limitations, substantially as claimed, as described in claim 7 including:

an external memory engine operationally connected to said analysis machine (Narad, col. 7, lines 63-67); and

a hash engine operationally connected to said analysis machine (Narad, col. 14, lines 52-53, col. 6, line 62 through col. 63, line 2).

10. Regarding claim 12, Cho teaches the limitations, substantially as claimed, as described in claim 10 including:

packet input global access bus software code used for flow of data packet information from a flexible input data buffer to an analysis machine (Narad, Fig. 2, col. 32, lines 1-7, col. 33, lines 64-67).

11. Regarding claims 13 and 18, Cho teaches the limitations, substantially as claimed, as described in claim 10 including:

results global access bus software code used for providing flexible access to an external memory (Narad, col. 36, lines 46-58).

12. Regarding claim 14, Cho teaches the limitations, substantially as claimed, as described in claim 10 including:

statistics data global access bus software code used for connection of an analysis machine to a packet manipulator (Narad, col. 8, lines 15-20, col 15, lines 21-22).

13. Regarding claim 15, Cho teaches the limitations, substantially as claimed, as described in claim 10 including:

private data global access bus software code used for connection of an analysis machine to an internal memory engine submodule (Narad, col. 12 ,line 50 through col. 13, line 13).

14. Regarding claim 16, Cho teaches the limitations, substantially as claimed, as described in claim 10 including:

lookup global access bus software code used for connection of an analysis machine to an internal memory engine submodule (Narad, col. 36, lines 40-45).

15. Regarding claim 17, Cho teaches the limitations, substantially as claimed, as described in claim 10 including:

results global access bus software code used for providing flexible access to an external memory (Narad, col. 36, lines 46-58).

16. Regarding claim 19, Cho teaches the limitations, substantially as claimed, as described in claim 10 including:

a bi-directional access port operationally connected to said analysis machine (Narad, col. 104, lines, 50-62);

a flexible data input buffer operationally connected to said analysis machine (Narad, col. 15, lines 14-18); and

a flexible data output buffer operationally connected to said analysis machine (Narad, col. 16, lines 26-30).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cho as applied to claims 1 and 6, in view of Islam et al. (U.S. Publication Number 2003/0035430 A1).

Regarding claim 5, Cho teaches the limitations, substantially as claimed, as described in claim 1. However, Cho does not explicitly state processing data at a rate of at least 10 Gbs. In an analogous art, Islam teaches a programmable network device (see Abstract), processing data at a rate of at least 10 Gbs (see Paragraph 43). Therefore it would have been obvious to a person with ordinary skill in the art at the time of the invention to have modified Cho to include processing data at a rate of 10 Gbs because it would enhance the processing speed of the data and reduce the processing time and the load on the data networks.

Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho as applied to claims 1 and 6, in view of Narad et al. (U.S. Patent Number 6,157,955) and Stuttard et al. (U.S. Publication Number 2002/0174318 A1).

17. Regarding claim 8, Cho and Narad teach the limitations, substantially as claimed, as described in claim 7. However, Cho and Narad do not explicitly state wherein said analysis machine is multi-threaded. In an analogous art, Stuttard teaches a parallel data processing apparatus (see Abstract), in which he teaches wherein the analysis machine is multi-threaded (see paragraphs 49-50). Therefore it would have been obvious to one in the ordinary skill in the art at the time of the invention to have modified Cho as modified, by teaching of Stuttard, because wherein the analysis machine is multi-threaded, would enable concurrent processing of multiple tasks simultaneously.

18. As to claim 9, Cho as modified, teaches wherein the analysis machine has 32 threads (see Stuttard, paragraph 153).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. Bret Dennison whose telephone number is (571)272-3910. The examiner can normally be reached on M-F 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David A Wiley can be reached on (703) 308-5221. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information

for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

J. Bret Dennison
Patent Examiner
Art Unit 2143

ZARNI MAUNG
SUPV EXAMINER